UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,474	12/01/2003	Masood Murtuza	TI-35639	5891

23494 7590 08/19/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
BAUMGARDNER, MARK A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/726,474	MURTUZA, MASOOD	
	Examiner	Art Unit	
	Mark A. Baumgardner	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *15-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/01/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, (Claims 1-14, drawn to a semiconductor device) in the reply filed on July 28, 2005 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Davis et al. (6,650,010).

With respect to Claim 1, Davis teaches the claimed semiconductor device comprising a substrate (substrate, Figure 5, #51), at least one inter-level dielectric (ILD) layer having a low dielectric constant (low-k dielectric layer, Figure 5, #69; column 5, lines 20-25), and at least one support structure disposed in the ILD layer (vias, Figure 5, #47) to mitigate damage of the semiconductor device caused by stresses to the ILD layer (column 5, lines 44-49).

With respect to Claim 3, Davis further teaches that the at least one support structure is one of a trench and via (vias, Figure 5, #47) formed from a support material (column 4, lines 40-44).

With respect to Claim 4, Davis further teaches that the support material comprises at least one of aluminum, aluminum alloy, copper, copper alloy, tungsten, or tungsten alloy (copper, column 5, line 59).

With respect to Claim 5, Davis further teaches that the support structure (vias, Figure 5, #47) mitigates damage of the ILD layer due to forces applied onto the ILD layer during one of a subsequent processing and packaging of the semiconductor device. Davis teaches the intended use of the support structure (column 2, lines 6-18 and 34-50) and further teaches that the vias (Figure 5, #47) provide the necessary vertical mechanical integrity (column 5, line 60), thereby mitigating damage of the ILD layer due to forces applied onto the ILD layer during one of a subsequent processing and packaging of the semiconductor device.

With respect to Claim 6, Davis further teaches that the semiconductor further comprises a plurality of low-k ILD layers (low-k dielectric material, Figure 5, #61 and low-k dielectric layers, Figure 5, #65 and #69) and at least one support structure disposed in each plurality of low-k ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to form a support column (vias, Figure 5, all designated by #47 overly each other to form a support column).

With respect to Claims 7 and 8, Davis further teaches that the support structures are located underneath the source of the stress, with the source of the stress being a bond pad location (metal pads, Figure 4, #45) to mitigate damage to the semiconductor device (column 4, lines 56-64).

With respect to Claim 9, Davis further teaches the at least one additional ILD layer (passivation layer, Figure 5, #73) having a dielectric constant which is higher than the low-k ILD

layer (Davis teaches use of silicon oxide or silicon nitride in column 5, lines 25-26, which inherently has a higher dielectric constant) overlying the at least one low-k inter-level dielectric layer (low-k dielectric layer, Figure 5, #69).

With respect to Claim 10, Davis further teaches the support column (vias, Figure 5, all designated by #47) ending at the one additional ILD layer (passivation layer, Figure 5, #73). Davis teaches that final metal layer (Figure 5, #71) comprises the metal lines (#37) and (#38) and metal pads (#45), shown in Figure 4. Hence, the support column ends at the one additional ILD layer.

With respect to Claim 11, Davis further teaches at least one support structure disposed in the at least one additional ILD layer. Again, Davis teaches that final metal layer (Figure 5, #71) comprises the metal lines (#37) and (#38) and metal pads (#45), shown in Figure 4. Hence, the at least one support structure is disposed in the at least one additional ILD layer.

With respect to Claims 12 and 14, Davis further teaches a plurality of support structures disposed in the at least one low-k dielectric layer (vias, Figures 4 and 5, all designated by #47) at a location below a bond pad (metal pads, Figure 4, #45) disposed on the semiconductor device in an n x m matrix configuration where n and m are integers greater than one (Figure 4 teaches a 3x3 matrix configuration).

With respect to Claim 13, Davis further teaches that that a plurality of support structures are disposed in the at least one low-k dielectric layer at a plurality of locations spaced equidistant apart from each other across substantially the entire layer. Figure 4 teaches equidistant spacing of a plurality of support structures (vias, Figure 4, all designated by #47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (6,650,010) in view of Davis et al. (6,650,010).

With respect to Claim 2, Davis teaches the invention set forth above in Figures 4 and 5, but lacks a teaching of the material in the Detailed Description pertaining specifically to those figures (column 4, line 36—column 5, line 65, inclusive). However, when teaching a manufacturing process of the invention (Figures 6A through 6H; column 5, line 66—column 6, line 65, inclusive), Davis teaches that is well known to use SiLK™ in at least one ILD layer (column 6, lines 8-10). SiLK™ material is known to have a dielectric constant (κ) less than 2.7; hence, an ultra-low dielectric constant is an inherent feature of SiLK™ material. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use SiLK™ in at least one ILD layer for the purpose of fabricating a higher speed and more dense semiconductor device (column 1, lines 34-37).

Conclusion

Non-Patent Document:

The examiner has referenced a non-patent document containing information pertaining to dielectric properties of SiLK™ and other materials (Clarke, Michael E. "Introducing Low-k

Dielectrics into Semiconductor Processing"). The full citation of this document is found in the Notice of References Cited.

Contact Information:

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Baumgardner. The examiner can normally be reached on Mon-Fri 9-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAB
8/15/2005

Zandra Smith
Primary Examiner